THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Previously Presented) A semiconductor storage device comprising:

a semiconductor layer;

a gate conductor formed on the semiconductor layer, said gate conductor consisting of a single gate electrode formed on the semiconductor layer with a gate insulation film disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions arranged on opposite sides of the channel region; and

memory function bodies formed on opposite sides of the gate electrode and having a function to retain electric charges, wherein

gate conductor functions for writing to, and erasing and reading from the semiconductor storage device are solely carried out with the single gate electrode.

2. (Previously Presented) A semiconductor storage device comprising:

a semiconductor layer;

a gate conductor formed on the semiconductor layer, said gate conductor consisting of a single gate electrode formed on the semiconductor layer with a gate insulation film disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions arranged on opposite sides of the channel region; and

two charge storage regions, each of the charge storage regions being in a shape of a film parallel to a surface of the semiconductor layer and existing over part of the channel region and part of the corresponding diffusion region, straddling a boundary therebetween, wherein

gate conductor functions for writing to, and erasing and reading from the semiconductor storage device are solely carried out with the single gate electrode.

3. (Previously Presented) A semiconductor storage device comprising:

a plurality of memory elements arranged along a word line,

wherein two memory function bodies having a function to retain electric charges are formed so as to extend along the word line on opposite sides of the word line,

each of the plurality of memory elements comprising:

a semiconductor layer;

a gate conductor formed on the semiconductor layer, said gate conductor consisting of a single gate electrode and comprising a part of the word line;

a gate insulation film formed between the semiconductor layer and the part of the word line;

a channel region arranged under the part of the word line;

diffusion regions arranged on opposite sides of the channel region; and

a part of each of the memory function bodies that exists over part of the channel region and part of the corresponding diffusion region, straddling a boundary therebetween, wherein

gate conductor functions for writing to, and erasing and reading from each memory element are solely carried out with the single gate electrode.

4. (Original) The semiconductor storage device as claimed in claim 3, wherein

the word line consists of a single word line,

the memory function bodies are arranged only on both sides of the single word line, and

the memory function bodies are each comprised of one or more insulative materials.

5. (Original) The semiconductor storage device as claimed in claim 4, wherein a word line to be selected when information is rewritten to the memory element is only the single word line.

6. (Original) The semiconductor storage device as claimed in claim 1, wherein

each of the memory function bodies is comprised of one or more insulative materials, and

at least part of each memory function body is formed so as to overlap with part of the corresponding diffusion region.

7. (Withdrawn) The semiconductor storage device as claimed in claim 1, wherein the semiconductor layer is comprised of a SOI layer.

8. (Withdrawn) The semiconductor storage device as claimed in claim 1, wherein the semiconductor layer includes a well region.

9. (Previously Presented) The semiconductor storage device as claimed in claim 1, wherein each of the memory function bodies includes a charge retention film having a function of storing electric charges, and an insulator.

10. (Previously Presented) The semiconductor storage device as claimed in claim 9, wherein the charge retention film includes a first portion that has a surface roughly parallel to a surface of the gate insulation film.

11. (Previously Presented The semiconductor storage device as claimed in claim 10, wherein the charge retention film includes a second portion extended roughly parallel to a side surface of the gate electrode.

12. (Previously Presented) The semiconductor storage device as claimed in claim 11, wherein the insulator includes an insulation film that separates the gate electrode from the second portion of the charge retention film extended roughly parallel to the side surface of the gate electrode.

13. (Previously Presented) The semiconductor storage device as claimed in claim 10, wherein the insulator includes an insulation film that separates the first portion of the charge retention film from the channel region or the semiconductor layer.

14. (Original) The semiconductor storage device as claimed in claim 13, wherein the insulation film that separates the first portion of the charge retention film from the channel region or the semiconductor layer has a film thickness, which is smaller than a film thickness of the gate insulation film and not smaller than 0.8 nm.

15. (Original) The semiconductor storage device as claimed in claim 13, wherein the insulation film that separates the first portion of the charge retention film from the channel region or the semiconductor layer has a film thickness, which is greater than a film thickness of the gate insulation film and not greater than 20 nm.

16. (Previously Presented) The semiconductor storage device as claimed in claim 1, wherein each diffusion region is effectively offset with respect to the gate electrode.

17. (Previously Presented) The semiconductor storage device as claimed in claim 3, wherein each diffusion region is effectively offset with respect to the word line.

18. (Withdrawn) The semiconductor storage device as claimed in claim 16, wherein each memory function body includes an insulation film formed on a remotest side from the gate electrode in order to secure a prescribed amount of offset of each diffusion region.

19. (Withdrawn) The semiconductor storage device as claimed in claim 17, wherein each memory function body comprises an insulation film formed on a remotest side from the word line in order to secure a prescribed amount of offset of each diffusion region.

20. (Previously Presented) Portable electronic equipment having the semiconductor storage device as claimed in claim 1.

21. (Withdrawn) The semiconductor storage device as claimed in claim 2, wherein the semiconductor layer is comprised of a SOI layer.

22. (Withdrawn) The semiconductor storage device as claimed in claim 2, wherein the semiconductor layer includes a well region.

23. (Previously Presented) The semiconductor storage device as claimed in claim 2, wherein each diffusion region is effectively offset with respect to the gate electrode.

24. (Withdrawn) Portable electronic equipment having the semiconductor storage device as claimed in claim 2.

25. (Withdrawn) The semiconductor storage device as claimed in claim 3, wherein the semiconductor layer is comprised of a SOI layer.

26. (Withdrawn) The semiconductor storage device as claimed in claim 3, wherein the semiconductor layer includes a well region.

27. (Previously Presented) The semiconductor storage device as claimed in claim 3, wherein each of the memory function bodies includes a charge retention film having a function of storing electric charges, and an insulator.

28. (Withdrawn) Portable electronic equipment having the semiconductor storage device as claimed in claim 3.

29. (Previously Presented) The semiconductor storage device as claimed in claim 1, wherein the gate electrode does not cover the memory function bodies.

30. (Previously Presented) The semiconductor storage device as claimed in claim 2, wherein the gate electrode does not cover the charge storage regions.

31. (Previously Presented) The semiconductor storage device as claimed in claim 3, wherein the word line does not cover the memory function bodies.